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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/008,515 | 11/08/2001 | Jay B. Reimer | TI-30113 | 5418 |

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| EXAMINER | |
|---|---|
| SONG, JASMINE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/008,515 | REIMER ET AL. |
| | Examiner | Art Unit |
| | Jasmine Song | 2188 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *8 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-18* is/are allowed.

6)☒ Claim(s) *1,2,5,6,12-15 and 19* is/are rejected.

7)☒ Claim(s) *3,4,7-11 and 20-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## Detailed Action

1. This office action is in response to Amendment A filed on 04/08/2004, claims 1-24 are still pending. All rejections and objections not explicitly repeated below are withdrawn.

## Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2,5-6,12-15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rao et al., US 6,253,293 B1, in view of Belhaj., US 6,564,179 B1.

Regarding claim 1, Rao et al teach that a digital signal processing system that comprises;

a shared data memory (Fig.2, a shared data RAM 204);

a plurality of processor subsystems (it is taught as DSPA 200a and DSPB 200b, each coupled to data RAM, program RAM, and program ROM, Fig.2) coupled to the shared memory (Fig.2) to concurrently access data stored by the shared data memory (col.10, lines 41-43 and Fig.4), wherein the shared data memory (Fig.2, a shared data RAM 204) is conditionally write-protected from at least one of the processor subsystems (col.10, lines 27-28 and col.11, lines 34-36 and Fig.4).

Rao does not teach a shared program memory which stored access instructions. He only teaches a shared data memory as disclosed above.

However, Belhaj teaches a shared program code memory (Fig.1, program code memory 104).

As taught by Belhaj, the use of the shared program code memory for two types of processors has the advantages of allowing the programmers program efficiently, and generate code easily and with minimum size requirements will be at a minimum (col.2, lines 18-21). It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Belhaj in the system of Rao and have the shared program code memory for two types of processors for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 2, Rao et al teach that the program memory and the plurality of processor subsystems are fabricated on a single chip (Fig.2).

Regarding claim 5, Rao et al teach that each of the plurality of processor subsystems includes:

a processor core (it is taught as DSPA 200a or DSPB 200b); and

an instruction bus (the line connected between program ROM and DSPA).

Regarding claim 6, Rao et al teach that each of said processor cores (it is taught as DSPA 200a or DSPB 200b) includes a bus interface module (the line connected between shared data RAM and DSPA) coupled to the associated instruction bus to access instructions stored by the shared program memory (Fig.2).

Regarding claim 12, Rao et al teach the processor subsystems each further include: data memory (Fig.2, 203a and 203b), wherein the processor core is configured to operate on data from the data memory in accordance with program instruction retrieved via the instruction bus (Fgi.2).

Regarding claim 13, Rao et al teach the processor subsystems each further include: a direct memory access controller (it is taught as data RAM 203 controller); and a memory bus (the line between shared data RAM and data RAM) that couples the DMA controller to the data memory (data RAM 203) and the shared data memory

(Fig.2, 204), wherein the memory bus is distinct from the instruction bus (the line between 202 and 200) and distinct from the data bus (the line between 203 and 200).

Regarding claim 14, Rao et al teach that the program memory is configured to service multiple instruction requests received via the instruction buses in each clock cycle (col.10, lines 41-43).

Regarding claim 15, Rao et al teach that the processor cores are configured to concurrently execute distinct instruction from a single program stored in the shared program memory, and wherein the order in which program instruction are executed by a processor core depends on the data that the processor core operates on (col.11, lines 34-44).

Regarding claim 19, Rao et al teach that a digital signal processor chip () that comprises:

a shared data memory (Fig.2, a shared data RAM 204); and

a plurality of processor cores (it is taught as DSPA 200a and DSPB 200b, Fig.2) coupled to the volatile memory (Fig.2) via a corresponding plurality of instruction buses (the lines connected between program ROM and DSP), and wherein each of the instruction buses is configured to convey only read operations to the volatile memory while their corresponding processor cores are in a normal operating mode (col.10, lines 27-28 and col.11, lines 34-36 and Fig.4).

Rao does not teach a shared program memory which stored access instructions. He only teaches a shared data memory as disclosed above.

However, Belhaj teaches a shared program code memory (Fig.1, program code memory 104).

As taught by Belhaj, the use of the shared program code memory for two types of processors has the advantages of allowing the programmers program efficiently, and generate code easily and with minimum size requirements will be at a minimum (col.2, lines 18-21). It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Belhaj in the system of Rao and have the shared program code memory for two types of processors for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

## Allowable Subject Matter

5. Claims16-18 are allowed.

6. Claims 3-4,7-11, 20-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

8. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Mano Padmanabhan 5/14/04

Jasmine Song

Patent Examiner

June 15, 2004

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100